REMARKS

Claims 1, 5-10, 26, 29, and 32-33 remain in the application. Claims 2-4, 11-25, 27, 28, and 30-31 have been cancelled.

By this amendment, applicants have amended claims 1 and 26 to more particularly set out the subject matter of the present invention in response to the present 35 U.S.C. §112 rejection. Additionally, claims 5-10, 29 and 32-33 have been amended to more appropriately depend from their respective independent claims.

Applicants respectfully submit that the present amendment complies with requirements of form set forth in the present Office Action, and that it further places the rejected claims in better form for consideration on appeal. Thus, applicants respectfully request its admission.

Response to the 35 U.S.C. §112 Rejection

Claims 1, 5-10, 26, 29 and 32-33 were rejected under §112, second paragraph because it was unclear whether the intermediate structure has the semiconductor (cap) layer being at least partially an oxide layer. By this amendment, applicants have amended claim 1 to include a polycrystalline semiconductor layer and claim 26 to include a polysilicon cap layer. Further applicants have amended claims 1 and 26 so that it is clearer what the intermediary structure is comprised of. Specifically, the language involving oxidizing has been removed from both claims so that it is clearer that the intermediary structure includes

the polycrystalline semiconductor layer (claim 1) or the polysilicon cap layer (claim 26). With these changes, applicants respectfully believe that claims 1, 5-10, 26, 29 and 32-33 are in compliance with §112, second paragraph.

## Response to Prior Art Rejections

Claims 1, 6-8, 26, 29 and 32 were rejected under 35 U.S.C. §102(e) as being anticipated by Mandelman, USP 6,518,641 ("Mandelman"). This rejection is respectively traversed in view of the amendments made herein and the remarks presented hereinafter.

Claim 1 now calls for an intermediary of a semiconductor device having, among other things, a polycrystalline semiconductor layer overlying a first dielectric layer. The polycrystalline semiconductor layer has a second opening that at least partially overlies a first opening in the first dielectric layer.

Applicants respectfully submit that Mandelman does not show or suggest such a polycrystalline semiconductor layer. The present Office Action points to element 35 in Mandelman to teach this element. However, element 35 comprises a CVD oxide layer (see Col. 5, lines 45-50), which is not a polycrystalline semiconductor layer. Further, there is no direct evidence or suggestion in Mandelman that element 35 or any portion thereof was initially any other material but the CVD oxide.

Thus, because Mandelman fails show or suggest at least this element, applicants respectfully submit that claim 1 is allowable.

Claims 6-8 depend from claim 1 and are believed allowable for at least the same reasons as claim 1.

Claim 26 now calls for an intermediary of a semiconductor device having, among other things, a polysilicon cap layer formed overlying a first dielectric material. The polysilicon cap layer has a second opening at least partially over a first opening in the first dielectric material.

Applicants respectfully submit that Mandelman does not show or suggest such a polysilicon cap layer. The present Office Action points to element 35 in Mandelman to teach this element. However, element 35 comprises a CVD oxide layer (see Col. 5, lines 45-50), which is not a polysilicon cap layer. Further, there is no direct evidence or suggestion that that element 35 or any portion thereof was initially any other material but the CVD oxide.

Thus, because Mandelman fails show or suggest at least this element, applicants respectfully submit that claim 26 is allowable.

Claims 29 and 32 depend from claim 26 and are believed allowable for at least the same reasons as claim 26.

Claims 5, 9-10, 27 and 33 were rejected under 35 U.S.C. §103 as being unpatentable over Mandelman.

Claim 5 depends from claim 1. As stated above, Mandelman does not show or suggest a polycrystalline semiconductor layer or a polysilicon layer formed as set forth in claim 1 or claim 5 respectively. Mandelman instead forms his void structure by depositing an oxide 40 directly into trench 34, and during that process a void 42 is formed. Applicants respectfully disagree with the Examiner's assertion that if would have been obvious to one

skilled in the art at the time of the invention to use a polycrystalline or a polysilicon layer to convert to a semiconductor oxide to simplify the process. Process simplification is not the primary intent of the present invention. Instead, a key objective of the present invention has to do with creating a device having a larger void volume compared to prior art structures such a Mandelman's, which in turn provides better isolation and lower substrate capacitance. Mandelman fails to even recognize the problem of maximizing void volume (as evidenced by his use of a deposited (CVD) TEOS oxide for layer 40), and further fails to show or suggest using a polysilicon semiconductor layer formed having a second opening overlying at least in part the first opening as set forth in claims 5 and 1. As stated in applicants' specification including paragraph [0027], the polysilicon or polycrystalline semiconductor layer functions, among other things, to promote a fast closure of the second recessed region when exposed to a thermal oxidizing environment because the polysilicon/polycrystalline semiconductor layer provides a more direct supply of silicon/semiconductor atoms to form the semiconductor oxide (e.g., $SiO_2$). This more direct supply of silicon/semiconductor atoms means the opening closes faster, which means less material is formed on the sidewalls of the second recess region during the oxidation process, which further means a void is formed with a larger volume. A larger void volume means better isolation and lower substrate capacitance, which is a key objective of the present invention. Mandelman fails to show or suggest such an intermediary structure as set forth in claim 5. He simply teaches a structure that has the same problems as

those described in applicants' specification including paragraph [0004] (e.g., voids with minimal or non-optimal volume). Thus, claim 5 is believed allowable for at least these reasons.

Claim 9 depends from claim 8 and is believed allowable for at least the same reasons as claims 8 and 1.

Claim 10 depends from claim 7 and is believed allowable for at least the same reasons as claims 7 and 1.

In view of the above, it is believed that the claims are allowable, and the case is now in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

Guy E. Averett et al.

Kevin B. Jackson
Attorney for Applicant(s)
Reg. No. 38,502
Tel. (602) 244-5306

ON Semiconductor
Law Dept./MD A700
P.O. Box 62890
Phoenix, AZ 85082-2890

Date: April 18, 2007